IN THE CLAIMS:

Please cancel claims 13 and 14. **Please also amend** claims 15-17 and 21 as shown in the complete list of claims that is presented below.

Claims 1-14 (cancelled).

15. (currently amended) The chopper comparator circuit of claim [[14]] 16, further comprising a switch connected between the first stage input node and the first stage output node.

~~16.~~ (currently amended) [[The]] A chopper comparator circuit, ~~of claim 14,~~ comprising:

a first input terminal for receiving an analog input signal;

a second input terminal for receiving a reference voltage;

a first switch for connecting the first input terminal to a switch node;

a second switch for connecting the second input terminal to the switch node;

a comparator circuit output terminal; and

circuitry connected between the switch node and the comparator circuit output terminal for comparing the analog input signal and the reference voltage, the circuitry comprising a first stage having a first stage input node and a first stage output node, the first stage including a gated inverter that is coupled to the first stage input node, and a first capacitor coupled between the switch node and the first stage input node,

wherein the gated inverter comprises a first logic circuit transistor of a first conductivity type and a second logic circuit transistor of a second conductivity type connected to the first logic circuit transistor at an intermediate connection node, the intermediate connection node being connected to the first stage output node, the first logic circuit transistor having a control electrode that is connected to the first stage input node and the second logic circuit transistor having a control electrode that is also connected to the first stage input node, the gated inverter additionally comprising a first current control transistor of the first conductivity type and a second current control transistor of the second conductivity type, the first current control transistor being

connected to the first logic circuit transistor and the second current control transistor being connected to the second logic circuit transistor, the first current control transistor having a control electrode and the second current control transistor having a control electrode, the gated inverter further comprising an inverter connected between the control electrodes of the first and second current control transistors,

wherein the first stage further includes another gated inverter that is coupled to the first stage input node, the another gated inverter comprising another first logic circuit transistor of the first conductivity type and another second logic circuit transistor of the second conductivity type connected to the another first logic circuit transistor at another intermediate connection node, the another intermediate connection node being connected to the first stage output node, the another first logic circuit transistor having a control electrode that is connected to the first stage input node and the another second logic circuit transistor having a control electrode that is also connected to the first stage input node, the another gated inverter additionally comprising another first current control transistor of the first conductivity type and another second current control transistor of the second conductivity type, the another first current control transistor being connected to the another first logic circuit transistor and the another second current control transistor being connected to the another second logic circuit transistor, the another first current control transistor having a control electrode and the another second current control transistor having a control electrode, the another gated inverter further comprising another inverter connected between the control electrodes of the another first current control transistors and the another second current control transistor, and

wherein the chopper comparator circuit further ~~comprising~~ comprises a first control power supply line that is connected to an input terminal of the inverter in the gated inverter and a second control power supply line that is connected to an input terminal of the another inverter in the another gated inverter, the first and second control power supply lines being maintained at different potentials.

17. (currently amended) The chopper comparator circuit, of claim [[13]] 16, wherein the circuitry further comprises a second stage having a second stage input node and a second stage output node, the second stage including an additional gated inverter

that is coupled to the second stage input node, and a second capacitor connected between the first stage output node and the second stage input node.

18. (previously presented) The chopper comparator circuit of claim 17, wherein the additional gated inverter comprises an additional first logic circuit transistor of the first conductivity type and an additional second logic circuit transistor of the second conductivity type connected to the additional first logic circuit transistor at an additional intermediate connection node, the additional intermediate connection node being connected to the second stage output node, the additional first logic circuit transistor having a control electrode that is connected to the second stage input node and the second logic circuit transistor having a control electrode that is also connected to the second stage input node, the additional gated inverter also comprising an additional first current control transistor of the first conductivity type and an additional second current control transistor of the second conductivity type, the additional first current control transistor being connected to the additional first logic circuit transistor and the additional second current control transistor being connected to the additional second logic circuit transistor, the additional first current control transistor having a control electrode and the additional second current control transistor having a control electrode, the additional gated inverter further comprising an additional inverter connected between the control electrodes of the first and second additional current control transistors.

19. (previously presented) The chopper comparator circuit of claim 18, wherein the second stage also includes a further gated inverter that is coupled to the second stage input node, the further gated inverter comprising a further first logic circuit transistor of the first conductivity type and a further second logic circuit transistor of the second conductivity type connected to the further first logic circuit transistor at a further intermediate connection node, the further intermediate connection node being connected to the second stage output node, the further first logic circuit transistor having a control electrode that is connected to the second stage input node and the further second logic circuit transistor having a control electrode that is also connected to the second stage input node, the further gated inverter additionally comprising a further first current

control transistor of the first conductivity type and a further second current control transistor of the second conductivity type, the further first current control transistor being connected to the further first logic circuit transistor and the further second current control transistor being connected to the further second logic circuit transistor, the further first current control transistor having a control electrode and the further second current control transistor having a control electrode, the further gated inverter additionally comprising a further inverter connected between the control electrodes of the further first current control transistors and the further second current control transistor.

20. (previously presented) The chopper comparator circuit of claim 19, further comprising a switch connected between the second stage input node and the second stage output node.

21. (currently amended) [[The]] A chopper comparator circuit ~~of claim 19,~~ comprising:

a first input terminal for receiving an analog input signal;

a second input terminal for receiving a reference voltage;

a first switch for connecting the first input terminal to a switch node;

a second switch for connecting the second input terminal to the switch node;

a comparator circuit output terminal; and

circuitry connected between the switch node and the comparator circuit output terminal for comparing the analog input signal and the reference voltage, the circuitry comprising a first stage having a first stage input node and a first stage output node, the first stage including a gated inverter that is coupled to the first stage input node, and a first capacitor coupled between the switch node and the first stage input node,

wherein the gated inverter comprises a first logic circuit transistor of a first conductivity type and a second logic circuit transistor of a second conductivity type connected to the first logic circuit transistor at an intermediate connection node, the intermediate connection node being connected to the first stage output node, the first logic circuit transistor having a control electrode that is connected to the first stage input node and the second logic circuit transistor having a control electrode that is also

connected to the first stage input node, the gated inverter additionally comprising a first current control transistor of the first conductivity type and a second current control transistor of the second conductivity type, the first current control transistor being connected to the first logic circuit transistor and the second current control transistor being connected to the second logic circuit transistor, the first current control transistor having a control electrode and the second current control transistor having a control electrode, the gated inverter further comprising an inverter connected between the control electrodes of the first and second current control transistors,

wherein the circuitry further comprises a second stage having a second stage input node and a second stage output node, the second stage including an additional gated inverter that is coupled to the second stage input node, and a second capacitor connected between the first stage output node and the second stage input node,

wherein the additional gated inverter comprises an additional first logic circuit transistor of the first conductivity type and an additional second logic circuit transistor of the second conductivity type connected to the additional first logic circuit transistor at an additional intermediate connection node, the additional intermediate connection node being connected to the second stage output node, the additional first logic circuit transistor having a control electrode that is connected to the second stage input node and the second logic circuit transistor having a control electrode that is also connected to the second stage input node, the additional gated inverter also comprising an additional first current control transistor of the first conductivity type and an additional second current control transistor of the second conductivity type, the additional first current control transistor being connected to the additional first logic circuit transistor and the additional second current control transistor being connected to the additional second logic circuit transistor, the additional first current control transistor having a control electrode and the additional second current control transistor having a control electrode, the additional gated inverter further comprising an additional inverter connected between the control electrodes of the first and second additional current control transistors,

wherein the second stage also includes a further gated inverter that is coupled to the second stage input node, the further gated inverter comprising a further first logic circuit transistor of the first conductivity type and a further second logic circuit transistor

of the second conductivity type connected to the further first logic circuit transistor at a further intermediate connection node, the further intermediate connection node being connected to the second stage output node, the further first logic circuit transistor having a control electrode that is connected to the second stage input node and the further second logic circuit transistor having a control electrode that is also connected to the second stage input node, the further gated inverter additionally comprising a further first current control transistor of the first conductivity type and a further second current control transistor of the second conductivity type, the further first current control transistor being connected to the further first logic circuit transistor and the further second current control transistor being connected to the further second logic circuit transistor, the further first current control transistor having a control electrode and the further second current control transistor having a control electrode, the further gated inverter additionally comprising a further inverter connected between the control electrodes of the further first current control transistors and the further second current control transistor, and

wherein the chopper comparator circuit further ~~comprising~~ comprises a first control power supply line that is connected to an input terminal of the additional inverter and a second control power supply line that is connected to an input terminal of the further inverter, the first and second control power supply lines being maintained at different potentials.

22. (previously presented) The chopper comparator circuit of claim 19, wherein the second stage output node is connected to the comparator circuit output terminal.